

The mechanism of instability on device's characteristics due to inter-metal dielectrics with low-k material and the modified process

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ABSTRACT

In this paper, the effects of backend process on device characteristic shift are explored. It had been found that the transistors with different inter-metal-dielectric (IMD) films (FSG vs. USG) have different performance. Moreover, more of the IMD layers will result in more of the electrical characteristic shifts. The shift is dominated by the interface state reduction. The model of plasma-enhanced hydrogen out-diffusion during IMD film deposition is proposed to explain the BEOL-related device shift. In order to relieve this effect of electrical characteristic shift, another alloy step by pure hydrogen (H₂) anneal is implemented after metal-1 etch and before the Via-1 deposition. It is found the electrical characteristics taken at metal-1 stage are very close to those taken at metal-6 with passivation step. In addition, there is no apparent hot carrier lifetime degradation with or without the pure hydrogen treatment.

Keywords: inter-metal-dielectric (IMD), back-end-of-line (BEOL), pure hydrogen, hot carrier

1. INTRODUCTION

In deep sub-micron ULSI technology, the interconnect-related RC delay will be more serious, which will lead to the circuit speed reduction even the transistors have very small parasitic capacitance. Therefore, the using of IMD film with low dielectric constant (low-K) is inevitable. Different to SOG or O₃-TEOS process used in the old process generation, the use of low-k dielectrics (ex. FSG) should be integrated with the other process steps to prevent the out diffusion of the fluorine (F), which will lead to the bubble generation and IMD film crack during the burn-in test. These additional process steps include the deposition of nitride or oxinitride. Therefore, the over-all side effects on device characteristics may be a concern, e.g. threshold voltage shift, reliability degradation. In addition, the SPICE model can not well fit the I-V curve when the product are processed to different metal layers. In this paper, we compare the performance differences of transistors with and without low-k dielectrics, and the differences of transistors processed to metal-1 or metal-6. Based on the experimental data, a model and a modified process are proposed to explain this phenomenon and improve the process stability.

2. EXPERIMENT

The devices used in this evaluation were fabricated using a standard CMOS logic process with six metal layers for the backend. The front-end included features such as shallow-trench isolation (STI), dual gate oxide process with 32Å for core transistors and 65Å for I/O transistors. After the gate oxidation, 2000Å undoped polysilicon was deposited and patterned, and then the shallow extension formation for the core devices and the lightly doped drain (LDD) formation for the I/O

devices are followed. In addition, all the devices were with RTA 1015°C 10sec source/drain annealing. For the backend process, Table-1 shows the brief backend process flow and the split conditions in this study. From IMD-1 to IMD-5, USG and FSG are deposited at different wafers, respectively. In addition, the wafers with pure H₂ anneal after M-1 etch is also compared. After the metal-6 deposition, all the wafers are covered with the PEOX and nitride for the passivation. After full process, the electrical characteristics were taken by the HP4071 semiconductor analyzer and the evaluation of hot carrier degradation was performed at bench measurement with HP4145B.

Table-1 Process steps and split conditions

Process Step	Split
M-1 etch	---
Alloy	None vs. 410°C (H ₂ +N ₂) anneal vs. 450°C (H ₂) anneal
IMD 1~6	FSG vs. USG
Passivation	---
Alloy	410°C (H ₂ +N ₂) anneal

3. RESULTS and DISCUSSION

A. Observance of the Accumulation Effects of IMD Layers

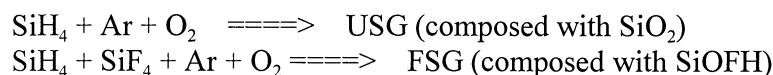
The BEOL-related device shifts are found to be with the accumulation effects when the IMD (old FSG) layers are increased, as shown in Fig. 1(a)-(b) for both of the NMOS and PMOS transistors. The I_{ds} increasing rate initially increases quickly, then slows down and finally saturates with the full process. This phenomenon is similar to that reported by D.Y.C. lie et al [1]. However, one can find that the increasing rate of PMOS transistor is smaller than that of NMOS transistors. This effect is also reported by D.Y.C. Lie et al.. But they attributed this difference to the PMOS was buried channel. On the contrary, the PMOS transistors were with surface channel in this study. Therefore, the effect on current increasing with more of the IMD layers for NMOS and PMOS transistors is really different.

To identify the possible mechanism, we perform the transconductance measurement. As shown in Fig. 2(a)-(b), the G_m % difference of NMOS transistors processed to M-1 and with full backend process is higher than that of PMOS transistors. From the C-V measurement, as shown in Fig. 3(a)-(b), the flatband shift for PMOS capacitors due to backend process is also smaller than that of NMOS transistors. So, one can conclude that the mobility increase can well explain the difference of current increase between NMOS and PMOS transistors. However, why the mobility increase in PMOS is smaller than NMOS is still not clear until now.

B. Comparison of USG and FSG

As shown in Fig. 1-3, one can observe that the IMD film with FSG has larger impact than that with USG film. Because all of the IMD-1~5 films are with FSG scheme which composes of large amount F atoms, it is very straightforward to consider that the device shift may be due to the F diffusion to oxide/Si interface. In addition, it had also been reported that when the atom fluorine (F) with high concentration was implanted or diffused to the oxide/Si interface, the mobility could be increased and the hot carrier degradation immunity depended on the F concentration [2]-[5]. In order to identify the role of F in the device shift, the composition of USG and FSG was compared. It can be observed that many of the F atoms can be released during deposition, as shown in the

following formula.



Because the USG film does not contain the F atoms during the process, if the assumption of F-enhanced the V_t shift and mobility increase is valid, then the transistors with USG should not be observed the electrical shift. However, from the experiment data, device's characteristics have also shifted, as shown in Fig. 1(a)-(b) for both of NMOS and PMOS transistors, respectively. It is found that the I_{dsat} increasing rate is higher for transistors with FSG IMD layers than that of transistors with USG IMD scheme, especially the process is with less IMD layer number. However, increasing the IMD layers with USG to Via-5 and metal-6, the increasing rate difference between FSG and USG is very little. In other words, the accumulation effect can also be observed for the transistors capped with USG film even it does not compose of the F atoms. In addition, comparing the C-V curves, it can be observed that there is no apparent difference of the inversion and accumulation capacitance, which means that the oxide thickness should not be changed. According to previous study of Wsix process on gate dielectrics by SLHsu [6], if there are high concentration F diffusion into oxide/Si interface, the oxide thickness should be increased about 10~15Å. However, it can not observe this phenomenon in this experiment. The only differences in the C-V curves are the flat-band shift and distortion. Base on above observance, it can be concluded that the device shift does not come from the F diffusion into oxide/Si interface. There should have the other mechanism, which dominates the device shift.

C. Hydrogen (H)-Enhanced Device Shift Model

To explain above phenomenon, the H-enhanced device shift model is proposed and verified by the Si data. The model is described as follows. It is well known that H^+ ions can be released during the PECVD nitride deposition [7]-[8]. In this study, the film of oxinitride (SINO) by PECVD is used as the bottom ARC for the Via layers. As a result, some of the H^+ ions can also diffuse to the oxide/Si interface. Because there are many of the dangling bonds have not been passivated during the front-end process. Therefore, these released H^+ ions can easily passivate these dangling bonds, then reduce the interface states and cause the device shift. More of the IMD layers lead to more of the SINO deposited, and more of the H atoms are released to passivate the interface states until all of the dangling bonds are passivated.

For the FSG film, which leads to higher I_{dsat} increasing rate, it can also be explained by the H-enhanced shift model. From the thermal degas (TDS) test not shown here, it is found that some of the H^+ ions can be released especially when the FSG is used. As a result, these H^+ ions released during FSG deposition and the H^+ ions released during SINO deposition can passivate more of the dangling bonds and lead to larger device shift.

4. MODIFIED PROCESS

In order to relieve the electrical difference between metal-1 stage and full process, the approach by pure H_2 anneal after meatl-1 etching was implemented. It is really found there is little difference for the nominal transistors (10/0.18) between metal-1 and metal-6, as shown in Table-2. There is another benefits with the pure H_2 anneal. Figure 4 shows the V_t roll-off characteristics of narrow width transistors. It can be found that the reverse narrow width effect can be relieved with H_2 annealing, especially for the PMOS transistors. This result can be explained as follows. Because most of the defects created during the trench etching can be passivated by the pure H_2 anneal, as a

result, the leakage currents from the side-wall of the active regions can be reduced.

There is one concern about the implement of pure H_2 anneal after metal-1 etch. That is the HCE lifetime degradation of I/O NMOS transistors with $V_{cc}=3.3V$. Figure 5 shows the HCE lifetime comparison of transistors with forming gas and pure H_2 anneal after meal-1 etching. There is about 2.5 times degradation for transistors with pure H_2 anneal. However, when the transistors are with full process, little difference can be observed.

Table-2 Electrical performance comparison at different process step

	M-1 with H_2 anneal	Full process
NMOS (W/L=10/0.18)	$V_{tl}=0.451V$, $I_{ds}=6.21mA$	$V_{tl}=0.445V$, $I_{ds}=6.31mA$
PMOS (W/L=10/0.18)	$V_{tl}=-0.475V$, $I_{ds}=-2.95mA$	$V_{tl}=-0.472V$, $I_{ds}=-3.01mA$

5. CONCLUSIONS

In this paper, the mechanism of BEOL-related device shift is explored. It is found FSG can induce larger shift than USG at the beginning metal layers (1~3). However, when the transistor is with the full process, little difference is observed. It reveals that the F atoms do not dominate the shift. To explain the device shift increase with the IMD layers, the H^+ -enhanced device shift model is proposed and verified well with the Si data. The H^+ ions can be released during any backend process, especially by PECVD process. These H^+ ions can passivate the dangling bonds in the oxide/Si interface. As a result, the threshold voltage can be reduced and the mobility can be increased. Finally, the I_{dsat} can be increased.

Based on the H^+ -enhanced device shift model, a modified process by pure H_2 anneal after metal-1 etching is also proposed to relieve the difference between transistors with one or two metal layers and with the full process. In addition, it is also observed that the reverse narrow width effect can be reduced. As for the H-enhanced HCE degradation, no apparent degradation can be observed after full process. In conclusion, the pure H_2 annealing before IMD-1 deposition can solve the issue of device shift coming from the backend process, and improve the other electrical characteristics.

5. REFERENCES

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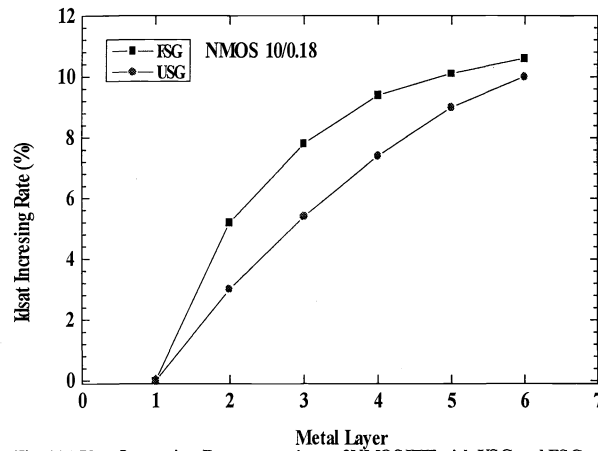


Fig. 1(a) Idsat Increasing Rate comparison of NMOSFET with USG and FSG.

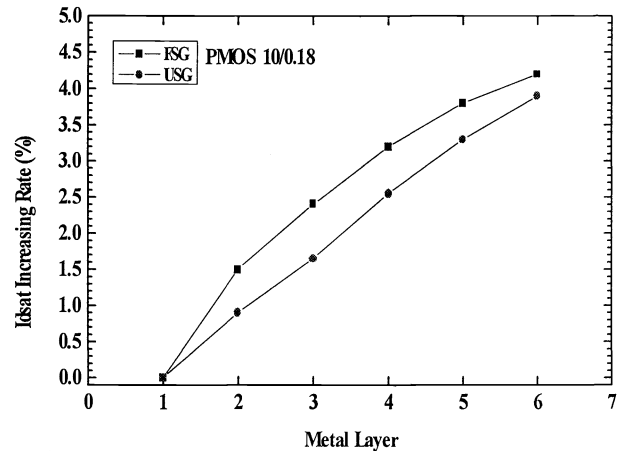


Fig. 1(b) Idsat Increasing Rate comparison of PMOSFET with USG and FSG.

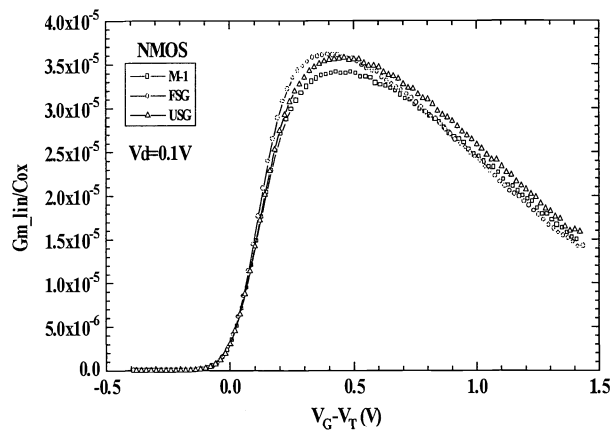


Fig. 2(a) Gm Increasing Rate comparison of NMOSFET with USG and FSG.

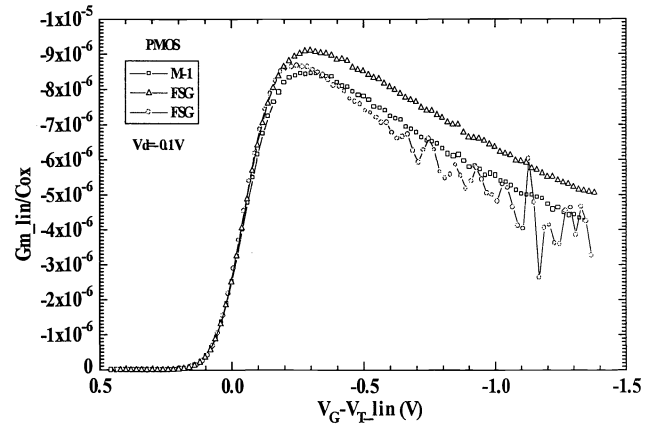


Fig. 2(b) Gm increasing rate comparison of PMOSFET with USG and FSG

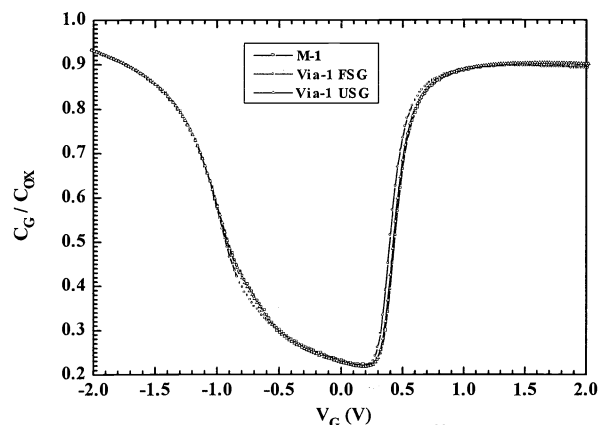


Fig. 3(a) Low frequency of NMOS Capacitor with different IMD layers

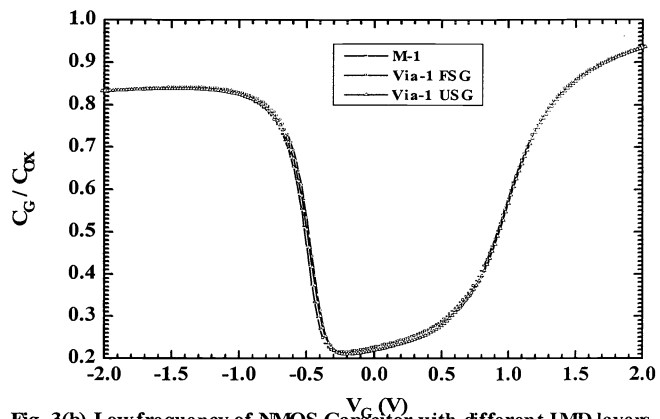


Fig. 3(b) Low frequency of NMOS Capacitor with different IMD layers

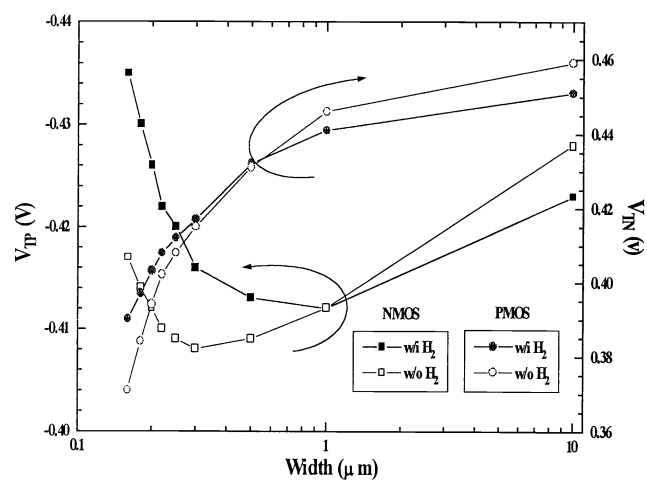


Fig. 4 Vt roll-off comparison of NMOS and PMOS with narrowwidth.

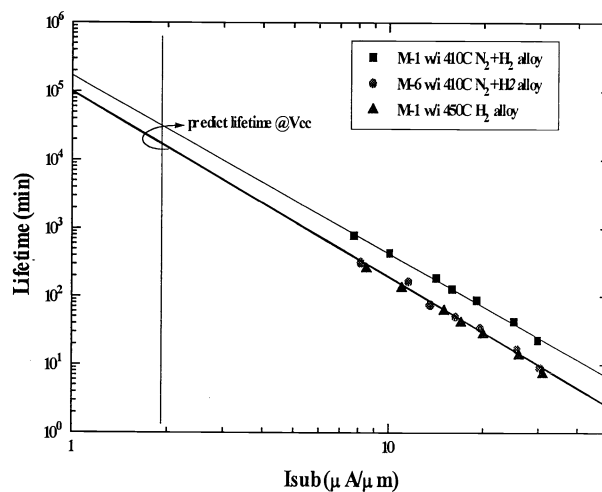


Fig. 5 Hot carrier degradation comparison of NMOS with different alloy gas.